

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (previously presented) A method comprising:
receiving an internal clock signal from a clock monitor of the self-timed memory;
receiving an external clock signal, wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal;
receiving a control signal;
providing, in dependence upon the control signal, the internal clock signal to at least one internal memory block during a normal mode of operation of the self-timed memory, and the external clock signal to the at least one internal memory block during a test mode of the self-timed memory, wherein providing the external clock signal to the at least one internal memory block comprises providing the external clock signal to a plurality of different internal memory blocks according to a predetermined test pattern;
and
detecting a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the internal memory block during the test-mode of the self-timed memory.
2. (canceled)
3. (previously presented) A method as defined in claim 1 wherein the duty cycle of the external clock signal received during test mode comprises a duty cycle lower than a 50% duty cycle typical for operation of the at least one internal memory block.

4. (previously presented) A method as defined in claim 1 wherein the duty cycle of the external clock signal received during test mode comprises a duty cycle higher than a 50% duty cycle typical for operation of the at least one internal memory block.
5. (previously presented) A method as defined in claim 1 further comprising providing the internal clock signal to the at least one internal memory block in an absence of the control signal.
6. (previously presented) A method as defined in claim 1 wherein receiving the control signal further comprises receiving a control signal indicating initiation of the test mode.
7. (previously presented) A method as defined in claim 6 wherein receiving the control signal further comprises receiving a control signal indicating termination of the test mode.
8. (previously presented) A method as defined in claim 7 wherein receiving the control signal further comprises receiving the control signal during the test mode.
9. (previously presented) A self-timed memory comprising:
 - at least one internal memory block;
 - a clock monitor for receiving an external clock signal and for providing a clock signal to the at least one internal memory block;
 - a test system interposed between the clock monitor and the at least one internal memory block, the test system comprising:
 - an internal clock signal input port in signal communication with the clock monitor for receiving an internal clock signal;
 - an external clock signal input port for receiving the external clock signal, wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal;
 - a control signal input port for receiving a control signal;

at least one output port in signal communication with the at least one internal memory block; and

a multiplexer in signal communication with the internal clock signal input port, the external clock signal input port, the control signal input port, and the at least one output port, wherein the multiplexer is configured to receive the internal clock signal, the external clock signal, and the control signal;

wherein the multiplexer is further configured to provide, in dependence upon the control signal, the internal clock signal via the at least one output port to the at least one internal memory block during a normal mode of operation of the self-timed memory, and the external clock signal to the at least one internal memory block during a test mode of the self-timed memory to detect a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the at least one internal memory block during the test mode of the self-timed memory, wherein providing the external clock signal to the at least one internal memory block comprises providing the external clock signal to different internal memory blocks according to a predetermined test pattern.

10. (original) A self-timed memory as defined in claim 9 wherein the clock monitor comprises an input port for receiving the external clock signal and wherein the input port is connected to the external clock signal input port of the test system.

11. (previously presented) A self-timed memory as defined in claim 10 comprising test circuitry in signal communication with the test system, the test circuitry for providing the control signal to the test system and for providing the external clock signal to the test system during the test mode.

12. (previously presented) A self-timed memory as defined in claim 9 wherein the at least one internal memory block comprises an address decoder.

13. (previously presented) A self-timed memory as defined in claim 9 wherein the at least one internal memory block comprises a sense amplifier.

14. (previously presented) A self-timed memory as defined in claim 9 wherein the at least one internal memory block comprises a column and bank decoder.

15. (previously presented) A self-timed memory as defined in claim 9 wherein the at least one internal memory block comprises a precharge and discharge circuitry.

16. (previously presented) A self-timed memory as defined in claim 9 wherein the at least one internal memory block comprises input/output latches.

17. (previously presented) A self-timed memory comprising:

- at least one internal memory block;

- a clock monitor for receiving an external clock signal and for providing a clock signal to the at least one internal memory block;

- a test system interposed between the clock monitor and the at least one internal memory block, the test system comprising:

- an internal clock signal input port in signal communication with the clock monitor for receiving an internal clock signal;

- an external clock signal input port for receiving the external clock signal, wherein the external clock signal comprises a duty cycle that is different from a duty cycle of the internal clock signal;

- a control signal input port for receiving a control signal;

- at least one output port in signal communication with the at least one internal memory block; and

- control circuitry in signal communication with the internal clock signal input port, the external clock signal input port, the control signal input port and the at least one output port, wherein the control circuitry is configured to receive the internal clock signal, the external clock signal, and the control signal;

- wherein the control circuitry is further configured to provide, in dependence upon the control signal, the internal clock signal via the at least one output port to the at least one internal memory block during a normal mode of

operation of the self-timed memory, and the external clock signal to the at least one internal memory block during a test mode of the self-timed memory to detect of a slow-to-rise delay or a slow-to-fall delay in response to providing the external clock signal to the at least one internal memory block during the test mode of the self-timed memory, wherein providing the external clock signal to the at least one internal memory block comprises providing the external clock signal to different internal memory blocks according to a predetermined test pattern.

18. (original) A self-timed memory as defined in claim 17 wherein the control circuitry comprises a multiplexer.
19. (previously presented) A self-timed memory as defined in claim 18 wherein the at least one internal memory block comprises an address decoder.
20. (previously presented) A self-timed memory as defined in claim 19 wherein the at least one internal memory block comprises a sense amplifier.
21. (previously presented) A self-timed memory as defined in claim 20 wherein the at least one internal memory block comprises a column and bank decoder.
22. (previously presented) A self-timed memory as defined in claim 21 wherein the at least one internal memory block comprises a precharge and discharge circuitry.
23. (previously presented) A self-timed memory as defined in claim 22 wherein the at least one internal memory block comprises input/output latches.
24. (previously presented) A self-timed memory as defined in claim 23 further comprising test circuitry in signal communication with the test system, the test circuitry for providing the control signal to the test system and for providing the external clock signal to the test system during the test mode.